Remarks:

Applicants (hereinafter, Applicant) hereby request reconsideration of the application.

Applicant acknowledges the Examiner's confirmation of receipt of the claim for priority (and a certified copy of the priority application (see page 1, Office action)) under 35 U.S.C. § 119(a)-(d).

Regarding the second paragraph on page 2 of the Office action, it is noted that a continuation application, but not a CPA, was filed.

Claims 1-25 are now in the application. Claims 1 and 10 have been amended. No new matter is believed to have been added. Claims 21-25 are *withdrawn from consideration*. Affirmation of the election is herewith made regarding the last paragraph on page 3 of the Office action.

In the fourth paragraph on page 4 of the above-identified Office action, the Examiner objected to the drawings (as being of poor quality). In response, Applicant encloses herewith a formal copy of each changed drawing (Figs. 2-5).

In the fifth paragraph on page 4 of the above-identified Office action, the Examiner objected to the specification because of two (2) informalities. The Examiner's suggested corrections have been made.

In the first paragraph on page 5 of the above-identified Office action, the Examiner objected to claim 10 because of an informality. The Examiner's suggested correction has been made. Amended claim 10 now recites--selectively removing the first and second spacer layers by wet-chemical etching--.

The above-noted changes to claim 10 are provided solely for cosmetic and/or clarificatory reasons. They are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In the second paragraph on page 5 of the above-identified Office action, claims 1-21 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner stated that claim 1 used a confusing term (spacer layer). As the Examiner stated, Applicant may be his or her own lexicographer. However, contrary to the Examiner's statement, the terms in the claims are not given a meaning repugnant to any usual meaning of

these terms. "Spacer layer" has been traditionally used to encompass the meaning of "separating layer" in claims of U.S. patents. These terms (which are given the same aforementioned meaning) may be found in claims of thousands of U.S. patents. The Examiner is requested to consult the Examiner's supervisor regarding the matter.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph. The above-remarks are provided solely for the purpose of explaining the present invention. They are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In the last paragraph on page 5 of the Office action, claims 1-2 and 4-20 have been rejected as being obvious over Chan et al. (U.S. Pat. No. 6,365,465) (hereinafter, "Chan") under 35 U.S.C. § 103.

In the seventh paragraph on page 9 of the Office action, claim 3 has been rejected as being obvious over Chan in view of Shimizu (U.S. Pat. No. 5,753,541) under 35 U.S.C. § 103.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia, a method for fabricating a double gate MOSFET, which comprises the steps of:

depositing a second spacer layer on the semiconductor layer structure and the first spacer layer;

completely embedding the semiconductor layer structure in the first and second spacer layers by patterning the first and second spacer layers;

depositing a second insulation layer on a structure formed of the first and second spacer layers;

applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; and

introducing a further electrically conductive material into the region of the removed spacer layers.

Accordingly, the *present invention* is directed to a method for fabricating a double gate MOSFET transistor. A semiconductor layer structure of a transistor channel is embedded in a spacer material, and is contact-connected by source and drain regions (which are filled into depressions that are etched on

opposite sides of the semiconductor layer structure). Next, the spacer material is etched out selectively, and is replaced by the electrically conductive gate electrode material.

The Chan reference discloses a method for forming a double-gate MOSFET transistor. The method utilizes a selective lateral epitaxial growth of silicon from an existing single crystal silicon MOSFET channel to form the source/drain regions. The source/drain regions are bounded by pre-defined dielectric boundaries and are thereby limited in size to the local source/drain regions.

The dielectric which bounds the selective epitaxial growth is used as a self-aligned implant mask for selectively forming the heavily doped source/drain regions. The dielectric is removed after the source/drain formation to form a suspended silicon channel. The gate insulator and the gate electrodes are subsequently formed to complete the MOSFET.

Accordingly, Applicant points out that there are differences between the fabrication method of the present invention and that of Chan. In the present invention, the first and second spacer layers are patterned such that the semiconductor layer structure remains *completely* embedded in the first and second spacer layers. The Examiner compares this feature of the *present invention* with Fig. 3A of Chan, and states that the

SOI layer 5 is *substantially completely* embedded in the oxide layers 1 and 6 and in the nitride layers 2 and 7. However, in Chan, the SOI layer 5 is not covered (by the oxide and nitride layers) at the *side surfaces*. See Fig. 3A, Chan.

In contrast, the respective feature of the *present invention* discloses that the channel forming layer 4A is completely embedded by the layers 3 and 5. See Fig. 4 of the instant application. Therefore, Applicant deleted the term "substantially" (from original claim 1) to indicate that the semiconductor layer structure is indeed *completely* embedded in the first and second spacer layers.

Neither does Shimizu overcome the *deficiencies* of Chan.

The reference numerals corresponding to the above-features are presented solely for illustrative purposes. They are not intended to narrow the scope of the claims for any reason whatsoever.

Clearly, the references do not show "depositing a second spacer layer on the semiconductor layer structure and the first spacer layer; *completely embedding the semiconductor layer structure in the first and second spacer layers by patterning the first and second spacer layers;* depositing a second insulation layer on a structure formed of the first and

second spacer layers; applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; and introducing a further electrically conductive material into the region of the removed spacer layers", as recited in claim 1 of the instant application (emphasis added).

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since the dependent claims 2-20 are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-25 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone counsel so that, if possible, patentable language can be worked out.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of $110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

Ven Ponugoti

Ven R. Ponugoti

For Applicant

Reg. No.51,052

VRP:cgm

December 9, 2002

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification:

The paragraph starting at page 10, line 23 and ending at page 11, line 25, is amended as follows:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 2 thereof, there is shown a so-called silicon on insulator [(SIO)] (SOI) starting substrate containing a substrate 1, such as an silicon wafer, to which are subsequently applied a first oxide layer 2, a first spacer layer 3 made of silicon nitride (SiN) and a semiconductor layer 4 being a silicon layer in the present case. Such a starting substrate can be fabricated by wafer bonding, for example, in that, separately from one another, an oxide layer is grown on a first silicon wafer and a nitride layer is grown on a second silicon wafer and the two silicon wafers are fixed to one another at the oxide and nitride layers by a wafer bonding method known per se in the prior art. Afterwards, during the process, the second silicon wafer has to be brought to the desired thickness by polishing and/or etching. As an alternative to the fabrication process, the structure shown in Fig. 2 can also be obtained by successive deposition of the

layer construction shown and by subsequent recrystallization, for example laser recrystallization of the silicon grown in polycrystalline form. However, it is also theoretically conceivable to leave the semiconductor layer 4 in the polycrystalline state with a small crystallite size or even in the amorphous state. Although the mobility is restricted to a relatively great extent in this state, the small volume of the channel region and the complete punch-through of the gate potential nonetheless give rise to the prospect of a feasible power of the component even in that case. During fabrication, the complex recrystallization method could then be dispensed with.

The paragraph starting at page 12, line 6 and ending at line 11, is amended as follows:

The rectangular region 4A is subsequently [overgrown] <u>covered</u> by a second spacer layer 5 made of SiN, with the result that it is completely enclosed by the SiN material, as is illustrated in Fig. 3. As will become evident further below, the SiN material serves as a spacer material for a gate electrode that is to be used in its place.

In the claims:

Claim 1 (amended). A method for fabricating a double gate MOSFET, which comprises the steps of:

providing a substrate structure having a silicon substrate layer, a first insulation layer disposed on the silicon substrate layer, a first spacer layer disposed on the first insulation layer, and a semiconductor layer disposed on the first spacer layer;

patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET;

depositing a second spacer layer on the semiconductor layer structure and the first spacer layer;

[patterning the first and second spacer layers such that the semiconductor layer structure remains substantially] completely <u>embedding the semiconductor layer structure</u> [embedded] in the first and second spacer layers <u>by patterning the first and second spacer layers</u>;

depositing a second insulation layer on a structure formed of the first and second spacer layers;

vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them, during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case;

filling the depressions with an electrically conductive material;

forming a contact hole in the second insulation layer;

selectively removing the first and second spacer layers through the contact hole made in the second insulation layer;

applying third insulation layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure; and

introducing a further electrically conductive material into the region of the removed spacer layers.

Claim 10 (amended). The method according to claim 1, which comprises [using a] selectively removing the first and second

spacer layers [acting,] by wet-chemical etching [step for removing the first and second spacer layers].